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Claims

[c1] 1. A method of reducing the effect of coupling on a reference signal due to a transition in an output signal generated by an output buffer on an output path, said method being performed in said output buffer, said method comprising:
inverting said output signal to generate an inverted signal; and
connecting said inverted signal through an impedance that stores an energy, said inverted signal being connected to a node at which said reference signal is received by said output buffer.

[c2] 2. The method of claim 2, wherein said impedance comprises a capacitor.

[c3] 3. The method of claim 2, wherein said output buffer is implemented using transistors
of a voltage specification of a first voltage level, said output signal is generated having a swing equaling a second voltage level, wherein said first voltage level is lower than said second voltage level.

[c4] 4. The method of claim 2, wherein a capacitance of said

capacitor equals the parasitic capacitance of a transistor connected between said node and said output path, said transistor being comprised in said output buffer.

[c5] 5. An output buffer generating an output signal having a swing equaling a first voltage level, said output buffer comprising:

a first transistor and a second transistor together operating as a first inverter, each of said first transistor and said second transistor being of a voltage specification of a second voltage level, wherein said second voltage level is lower than said first voltage level;

a third transistor (320-A) and a fourth transistor protecting said first transistor and said second transistor from exposure to said first voltage level,

wherein each of said first transistor, said second transistor, said third transistor, and said fourth transistor contains a source terminal, a drain terminal, and a gate terminal,

the source terminal of said third transistor is coupled to the drain terminal of said first transistor at a fourth node, the gate terminal of said third transistor is coupled to a reference voltage at a first node, the drain terminal of said third transistor is coupled to the drain terminal of said fourth transistor,

the source terminal of said fourth transistor is coupled

to the drain terminal of said second transistor at a fifth node, the gate terminal of said fourth transistor is coupled to said reference voltage at a second node,
the gate terminal of said first transistor is coupled to receive a first input swing signal,the gate terminal of said second transistor is coupled to receive a second input swing signal, each of said first input swing signal and said second input swing signal having a lower swing than said first voltage level, the source terminal of said second transistor is coupled to receive a ground voltage, the source terminal of said first transistor is coupled to receive a supply voltage of said first voltage level,
a parasitic capacitance of said third transistor and said fourth transistor coupling said output signal to said first node and said second node respectively; and
a second inverter, a first capacitor, and a second capacitor together countering the effect of coupling of said output signal to said first node and to said second node, said second inverter generating an inverted signal of said output signal at a sixth node, said first capacitor connecting said inverted signal to said first node, and said second capacitor connecting said inverted signal to said second node.

[c6] 6. The output buffer of claim 5, wherein said second inverter comprises:

a fifth transistor (310-B) and a sixth transistor (325-B) together performing an inverting operation on said output signal; and

a seventh transistor and a eighth transistor protecting said fifth transistor and said sixth transistor from exposure to said first voltage level,

wherein said fifth transistor, said sixth transistor, said seventh transistor and said eighth transistor is of a voltage specification of said second voltage level, each of said fifth transistor, said sixth transistor, said seventh transistor, and said eighth transistor contains a source terminal, a drain terminal, and a gate terminal,

the source terminal of said seventh transistor is coupled to the drain terminal of said fifth transistor, the gate terminal of said seventh transistor is coupled to said first node, the drain terminal of said seventh transistor is coupled to the drain terminal of said eighth transistor at said sixth node, the source terminal of said fifth transistor is coupled to receive said supply voltage,

the source terminal of said eighth transistor is coupled to the drain terminal of said sixth transistor, the gate terminal of said eighth transistor is coupled to said second node, the source terminal of said sixth transistor is coupled to receive a ground voltage, the gate terminal of said fifth transistor is coupled to said fourth node, the gate terminal of said sixth transistor is coupled to said

fifth node.

[c7] 7. The output buffer of claim 6, further comprises:
a first resistor and a second resistor connected in series to operate as a potential divider network to generate a source reference voltage at a seventh node;
a third resistor connected between said seventh node and said first node to provide said source reference voltage as said reference voltage at said first node; and
a third resistor connected between said seventh node and said second node to provide said source reference voltage as said reference voltage at said second node.

[c8] 8. The output buffer of claim 7, further comprises:
a fifth resistor connected between the drain terminal of said third transistor and an output path; and
a sixth resistor connected between the drain terminal of said fourth transistor and said output path, wherein each of said fifth resistor and said sixth resistor provides linear impedance to reduce jitter in said output signal.

[c9] 9. The output buffer of claim 8, wherein each of said first transistor, said third transistor, said fifth transistor and said seventh transistor comprises a PMOS transistor, and each of said second transistor, said fourth transistor, said sixth transistor and said eighth transistor comprises a NMOS transistor.

[c10] 10. The output buffer of claim 9, wherein each of said reference voltages provided to said first node and said second node approximately equals half of said first voltage level.

[c11] 11. The output buffer of claim 5, wherein a capacitance of said first capacitor equals the parasitic capacitance of said third transistor and a capacitance of said second capacitor equals the parasitic capacitance of said fourth transistor.

[c12] 12. An article of manufacture processing input data, said article of manufacture comprising:
a core module performing operations on said input data to generate a core output;
a pre-driver receiving said core output to generate a first swing signal and a second swing signal, each having a swing lower than a first voltage level; and
a pad driver generating an output signal of said first voltage level, said pad driver comprising:
a first transistor and a second transistor together operating as a first inverter, each of said first transistor and said second transistor containing a source terminal, a gate terminal and a drain terminal, the gate terminal of said first transistor receiving said first swing signal and the gate terminal of said second transistor receiving said

second swing signal, each of said first transistor and said second transistor being of a voltage specification of a second voltage level;

a third transistor and a fourth transistor protecting said first transistor and said second transistor from exposure to said first voltage level, each of said third transistor and said fourth transistor containing a source terminal, a gate terminal and a drain terminal, the gate terminal of each of said third transistor and said fourth transistor being coupled to receive a reference signal, a parasitic capacitance of said third transistor and said fourth transistor coupling said output signal to said reference signal; and

a second inverter and a first capacitor together countering the effect of coupling of said output signal to said reference signal, said second inverter generating an inverted signal of said output signal, said first capacitor connecting said inverted signal to said reference signal.

[c13] 13. The article of manufacture of claim 12, wherein a source reference signal is coupled as said reference signal to each of the gate terminal of said third transistor and the gate terminal of said fourth transistor, wherein said first capacitor couples said inverted signal to the gate terminal of said third transistor and a second capacitor couples said inverted signal to the gate terminal

of said fourth transistor.

[c14] 14. The article of manufacture of claim 13, wherein a capacitance of said first capacitor equals the parasitic capacitance of said third transistor and a capacitance of said second capacitor equals the parasitic capacitance of said fourth transistor.

[c15] 15. The article of manufacture of claim 14, wherein each of said first transistor and said third transistor comprises a PMOS transistor, and each of said second transistor and said fourth transistor comprises a NMOS transistor.

[c16] 16. The article of manufacture of claim 15, wherein each of said reference voltages provided to the gate terminal of said third transistor and the gate terminal of the fourth transistor approximately equals half of said first voltage level.

[c17] 17. An apparatus reducing the effect of coupling on a reference signal due to a transition in an output signal having a swing of a first voltage level, said apparatus comprising:
an input interface module providing an interface to receive an input signal;
an output interface module providing said output signal on an output node;

a processing logic generating said output signal in response to said input signal, said processing logic comprising:

means for generating an inverted signal based on said output signal; and

means for connecting said inverted signal through an impedance that stores an energy, said inverted signal being connected to a node at which said reference signal is received.

[c18] 18. The apparatus of claim 17, wherein said impedance comprises a capacitor.

[c19] 19. The apparatus of claim 18, wherein said output signal is generated by an output buffer on an output path, said output buffer is implemented using transistors of a voltage specification of a second voltage level, wherein said second voltage level is lower than said first voltage level.

[c20] 20. The apparatus of claim 19, wherein a capacitance of said capacitor equals the parasitic capacitance of a transistor connected between said node and said output path, said transistor being comprised in said output buffer.